Attorney Docket # 10003787-1

overlying ferroelectric isolation layer having at least one via extending therethrough. [wherein] the via [s of the ferroelectric isolation layer] being laterally sized larger than the corresponding contact via [s] aligned therewith, a first metal layer disposed over the ferroelectric device level, and an inter-level dielectric level disposed over the first metal level; and a second metal disposed over the inter-level dielectric level.

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- 40. (Previously Added) An integrated circuit, as defined in claim 39, wherein the contact vias are filled with tungsten contact plugs.
- 41. (Previously Added) An integrated circuit, as defined in claim 40, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

Claims 42 - 56 (Cancelled)

57. (Currently Amended) A method of forming an integrated circuit [, as defined in claim 54] comprising:

forming a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having at least one contact via extending therethrough;

forming a ferroelectric device level over the transistor isolation layer, the ferroelectric layer including at least one ferroelectric capacitor:

forming a first metal layer over the ferroelectric device level:

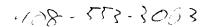
forming an inter-level dielectric level over the first metal layer:

forming a second metal level over the inter-level dielectric level; and

overlying ferroelectric isolation layer having at least one via extending

therethrough, wherein the via [s of the ferroelectric isolation layer] being laterally sized larger than the corresponding contact via [s] aligned therewith.

58. (Previously Presented) A method of forming an integrated circuit, as defined in claim 57, wherein the contact vias are filled with tungsten contact plugs.



Attorney Docket # 10003787-1



59. (Previously Presented) A method of forming an integrated circuit, as defined in claim 58, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

Claims 60-70 (Cancelled)